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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/700,391	11/04/2003	Arun Radhakrishnan	5500-91300	5786
53806	7590	03/06/2006		
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EXAMINER
CODY, DILLON J

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 03/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/700,391	Applicant(s) RADHAKRISHNAN ET AL.	
	Examiner Dillon Cody	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 November 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>2 February 2005</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-24 are pending.

Papers Filed

2. Examiner acknowledges receipt of claims, disclosure, drawings, and declaration, all filed 4 November 2003 and information disclosure statement filed 2 February 2005.

Title

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

5. Claim 10 is objected to because of the following informalities:

It is unclear which two opcodes are eligible to be selected from for the floating point operation stored in the cache. Applicant has not disclosed the floating point operation containing more than one opcode. For purposes of

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examination, examiner will interpret the claim to read "...configured to store a selected opcode for the floating point operation..."

Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 2-5 and 17-19 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 2 and 19 dictate predicting execution latency based upon a *predicted* precision of operands. The examiner asserts that operands' precisions are known at the time of execution based on whether they are single, double or extended-precise operands. There is no prediction required to obtain this information. The specification is silent as to a system requiring precisions to be predicted and how such a prediction is made. The examiner notes that the latency for a given precision of operands can be predicted. For purposes of examination, the examiner will interpret claims 2 and 17 to read "...responsive to a predicted precision latency of the operands..."

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8. Claims 3-5 and 18-19 are rejected on the basis of their dependencies to claims 2 and 17. Claims 5 and 19 shall be interpreted to read "...operands of the floating point operation has a latency that exceeds the predicted precision latency." Other references to "predicted precision" shall be interpreted as "predicted precision latency".

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1, 6-8, 13, 14, 16, 20, 22 and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Kahle et al. (U.S. Patent No. 5,802,386) hereinafter referred to as Kahle.

11. As per claim 1, Kahle discloses a processor comprising:

a prediction circuit configured to predict an execution latency of a floating point operation; *The examiner asserts that the processor contains circuitry to predict how long an instruction must wait before execution and uses said prediction in order to schedule said instruction. (Col. 5 lines 24-32)*

and a floating point unit coupled to receive the floating point operation for execution, wherein the floating point unit is configured to detect a misprediction of the

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execution latency. *Kahle discloses a floating point unit in his execution core (Col. 4 line 12). The examiner asserts that if an execution latency is mispredicted, the execution core will inherently detect the misprediction by not executing the instruction until all operands are available. If the execution core did not detect that the operands were not yet ready, then the processor may produce undesired results.*

12. As per claim 6, Kahle discloses the processor as recited in claim 1 further comprising a scheduler (Fig. 2 scheduler 230 and dispatch unit 240) coupled to the floating point unit (Fig. 2 execution unit 250), wherein the scheduler is configured to schedule the floating point operation for execution by the floating point unit, and wherein the floating point unit is configured to signal the scheduler responsive to detecting the misprediction. *The examiner asserts that if an instruction cannot execute because its operands are not yet ready, the scheduler must inherently halt issuance of subsequent instructions. (Col. 3 lines 54-56)*

13. As per claim 7, Kahle discloses the processor as recited in claim 6 wherein the scheduler is configured to reschedule the floating point operation responsive to the signaling from the floating point unit with the execution latency indicated as a latency detected by the floating point unit. *The examiner asserts that an instruction whose operands are not ready at a first time of execution is held in the execution unit until said operands are ready and is executed at a second time of execution. The second time of execution constitutes the rescheduled operation.*

14. As per claim 8, Kahle discloses the processor as recited in claim 6 wherein the prediction circuit is configured to predict the execution latency of the floating point operation responsive to dispatch of the floating point operation to the scheduler. *The examiner asserts that the amount of time the instruction waits in dispatcher 240 for operands to be ready before executing is calculated starting at the moment it leaves the scheduler 230 and arrives at dispatcher 240.*

15. As per claim 13, Kahle discloses the processor as recited in claim 1 wherein the floating point unit is configured to detect the misprediction responsive to detecting an actual execution latency greater than the execution latency predicted by the prediction circuit. *The examiner asserts that if the actual time until the operands are ready is longer than the predicted time, the instruction will have been issued to the floating point unit (Col. 5 lines 23-33). The misprediction is detected upon arrival at the floating point unit when the operands are not yet ready. If no such detection were made, the floating point unit would produce undesired operation.*

16. As per claim 14, Kahle discloses the processor as recited in claim 13 wherein the floating point unit is configured not to detect the misprediction responsive to detecting the actual execution latency is less than the execution latency predicted by the prediction circuit. *The examiner asserts that if the time until the operands are ready for execution of an instruction is less than the predicted time, that instruction will not have*

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yet been issued for execution. Since the instruction will arrive along with the already-ready operands, no misprediction will be detected. (Col. 5 lines 13-33).

17. As per claim 16, Kahle discloses a method performed by the processor described in claim 1. Therefore, claim 16 is rejected under the same grounds as claim 1 above.

18. As per claim 20, Kahle discloses a method performed by the processor described in claim 7. Therefore, claim 20 is rejected under the same grounds as claim 7 above.

19. As per claim 22, Kahle discloses a method performed by the processor described in claim 13. Therefore, claim 22 is rejected under the same grounds as claim 13 above.

20. As per claim 23, Kahle discloses a method performed by the processor described in claim 14. Therefore, claim 23 is rejected under the same grounds as claim 14 above.

21. Claims 1, 13, 15, 16, 22 and 24 are rejected under 35 U.S.C. 102(a) as being anticipated by Hammarlund (U.S. Publication No. US 2003/0126406) hereinafter referred to as Hammarlund.

22. As per claim 1, Hammarlund discloses a processor comprising:
a prediction circuit configured to predict an execution latency of a floating point operation; *The examiner asserts that the processor contains circuitry to predict how*

long an instruction must wait before execution and uses said prediction in order to schedule said instruction. (Paragraph 33 lines 7-9 and paragraph 34)

and a floating point unit coupled to receive the floating point operation for execution, wherein the floating point unit is configured to detect a misprediction of the execution latency. *Hammarlund discloses a floating point unit in his execution unit (paragraph 34 line 30). The examiner asserts that when an instruction is assigned to a delay slot after failing to execute a first time, a prediction is made as to how long it must wait before resources are available for a subsequent attempt at execution.*

23. As per claim 13, Hammarlund discloses the processor as recited in claim 1 wherein the floating point unit is configured to detect the misprediction responsive to detecting an actual execution latency greater than the execution latency predicted by the prediction circuit. *The examiner asserts that if the execution latency of the instruction was mispredicted, and the operand's resources are not all ready at the predicted time of execution, the instruction will be reassigned to a delay slot (Fig. 3 queues 332-338).*

24. As per claim 15, Hammarlund discloses the processor as recited in claim 13 wherein the floating point unit is further configured to detect the misprediction responsive to detecting the actual execution latency is less than the execution latency predicted by the prediction circuit. *The examiner asserts that if an instruction has been assigned to a delay slot it has been predicted to have a latency of M clock cycles, as is*

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assigned to that delay slot. If the results are available before the M cycles are up, the misprediction is detected and the operation is issued back for execution. (Paragraph 46 lines 6-10)

25. As per claim 16, Hammarlund discloses a method performed by the processor described in claim 1. Therefore, claim 16 is rejected under the same grounds as claim 1 above.

26. As per claim 22, Hammarlund discloses a method performed by the processor described in claim 13. Therefore, claim 22 is rejected under the same grounds as claim 13 above.

27. As per claim 24, Hammarlund discloses a method performed by the processor described in claim 15. Therefore, claim 24 is rejected under the same grounds as claim 15 above.

Claim Rejections - 35 USC § 103

28. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

29. Claims 2-5 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kahle in view of Markstein et al. (U.S. Patent No. 5,631,859) hereinafter referred to as Markstein.

30. As per claim 2, Kahle discloses the processor as recited in claim 1 wherein the prediction circuit is configured to predict the execution latency of a floating point operation but does not take into account the precision of operands of the floating point operation.

31. Markstein discloses a floating point unit capable of operating on variable-precision operands. (Col. 6 lines 10-18) *The examiner asserts that when a first instruction is waiting for an operand of a previous instruction, the execution latency of the first instruction depends on when operand(s) will be made available by the previous instruction. Operands with increased precision inherently take longer to calculate due to the larger number of bits involved in the operation.*

32. Markstein discloses his invention to be "an improved technique for allowing high precision calculations without slowing lower precision calculations" (Col. 2 lines 40-42) which is a desired outcome of Kahle.

33. It would have been obvious to one of ordinary skill in the art at the time of invention to have included Markstein's FPU in place of Kahle's for the benefit of higher precision calculations without slowing existing operations.

34. As per claim 3, Kahle and Markstein disclose the processor as recited in claim 2 wherein the floating point unit comprises a control register storing a precision control indication indicative of an output precision for floating point operation, wherein the predicted precision latency is the output precision. *Markstein discloses the ALU performing quad-precision arithmetic operations on quad-precision operands (Col. 6 lines 13-15) and double-precision operations on double-precision operands. The ALU must inherently contain logic to discern between the two in order to produce both types of output.*

35. As per claim 4, Kahle and Markstein disclose the processor as recited in claim 2 wherein the floating point operation is a multiply operation (Markstein col. 6 line 12), and wherein the floating point unit comprises a multiplier designed for a first precision less than a maximum precision supported by the processor, and wherein the execution latency is based on a number of passes through the multiplier used to complete a multiplication of the precision of the operands. (Col. 6 lines 13-15) *The examiner asserts that if a double-precise operation takes a given amount of time, doing that same operation twice will yield an execution latency of at least twice that of the double-precise operation.*

36. As per claim 5, Kahle and Markstein disclose the processor as recited in claim 2 wherein the floating point unit comprises a precision check circuit coupled to receive the operands of the floating point operation, wherein the precision check circuit is

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configured to detect the misprediction if at least one of the operands of the floating point operation has a [latency] that exceeds the predicted precision latency. *The examiner asserts that an operation inherently cannot execute if not all operands are ready. If it were to do so, undesired results may occur. The ALU must inherently contain circuitry (precision check circuit) to ensure this does not happen.*

37. As per claim 17, Kahle and Markstein disclose a method performed by the processor described in claim 2. Therefore, claim 17 is rejected under the same grounds as claim 2 above.

38. As per claim 18, Kahle and Markstein disclose a method performed by the processor described in claim 4. Therefore, claim 18 is rejected under the same grounds as claim 4 above.

39. As per claim 19, Kahle and Markstein disclose a method performed by the processor described in claim 5. Therefore, claim 19 is rejected under the same grounds as claim 5 above.

40. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kahle.

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41. As per claim 9, Kahle discloses the processor as recited in claim 6 further comprising a cache configured to store an indication of the execution latency predicted by the prediction circuit. (Col. 6 lines 22-24) Kahle fails to disclose the cache being a trace cache.

42. Official notice is taken that trace caches are extremely well known in the art.

43. Trace caches store commonly used strings (or traces) of operations in order of execution for the benefit of more easily recalling said traces for subsequent execution. This benefit is in line with a desired outcome of Kahle's invention of reusing common code (Col. 6 lines 22-29) and storing it with scheduling data.

44. It would have been obvious to one of ordinary skill in the art at the time of invention to have included a trace cache in place of the cache specified by Kahle in col. 6 lines 22-24 for the benefit of saving commonly used execution traces to speed up execution.

45. As per claim 10, Kahle discloses the processor as recited in claim 9 wherein the trace cache is configured to store a selected opcode of at least two opcodes for the floating point operation responsive to the execution latency predicted by the prediction circuit, the selected opcode comprising the indication of the execution latency. *The examiner asserts that the stored opcode comprises the scheduling data stored in the cache (Col. 6 lines 22-24). This scheduling data can take any form to represent the instruction latency data described by Kahle in col. 5 lines 13-33.*

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46. Claims 11-12 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kahle in view of Hammarlund et al. (U.S. Publication No. US 2003/0126406) hereinafter referred to as Hammarlund.

47. As per claim 11, Kahle discloses the processor as recited in claim 1 but fails to disclose wherein the floating point unit is configured to signal an exception responsive to detecting the misprediction.

48. Hammarlund discloses floating point unit (Fig. 3 execution unit 306) is configured to signal an exception responsive to detecting the misprediction. (Paragraph 4 lines 7-8) *The examiner asserts that Hammarlund's "correction routine" constitutes an exception.*

49. Hammarlund's invention provides a method of temporarily halting execution of instructions which cannot finish at this time. This provides the benefit of freeing execution logic from waiting for operands and allowing it to execute other instructions while waiting. This provides for faster execution of programs.

50. It would have been obvious to one of ordinary skill in the art at the time of invention to have included Hammarlund's rescheduling technique in Kahle's processor for the benefit of faster processing.

51. As per claim 12, Kahle and Hammarlund disclose the processor as recited in claim 11 wherein the processor is configured to refetch the floating point operation responsive to the exception. (Hammarlund paragraph 23)

52. As per claim 21, Kahle and Hammarlund disclose a method performed by the processor described in claim 12. Therefore, claim 21 is rejected under the same grounds as claim 12 above.

Conclusion

53. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hinton et al. (U.S. Patent No. 5,842,036) disclose a scheduling system taking into account predicted execution latencies of prior instructions.

54. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

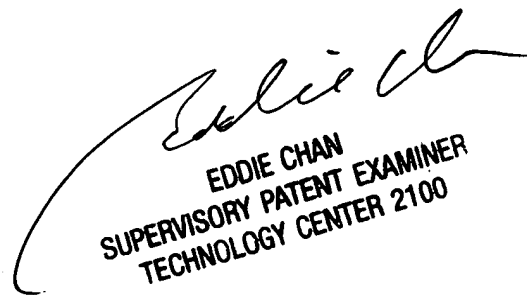
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dillon Cody whose telephone number is 571-272-8401. The examiner can normally be reached on Mon - Fri, 8 AM - 5 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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